ABSTRACT

A probe card assemblage for simultaneously testing one or more integrated circuit chips including an interposer having on one surface a plurality of protruding contact elements for electrically contacting one or more chips of a wafer positioned atop a layer of compliant material, and arrayed in a pattern corresponding to a chip pads, a series of conductive vias through the electrically insulating interposer which connect the chip contact elements with an arrangement of leads terminating in a universal arrangement of connectors on the second surface, and a probe card with connectors mating to those on the interposer. The connectors on the interposer is secured are secured to those on the probe card, thereby providing a vertical probe assemblage which makes use of ultrasonic energy to minimize scrub or over travel. The universal probe card is specific to a tester configuration and common to a family of circuits to be tested.